Amendments to the Claims

1. (previously presented): A high frequency integrated circuit structure comprising:

a body of semiconductor material having a plurality of isolated active regions, and comprising a first conductivity type;

internal circuitry formed in a first active region;

a second active region comprising a buried layer of a second conductivity type formed over the body of semiconductor material and a first semiconductor layer of the second conductivity type formed over the buried layer, wherein the first semiconductor layer has a lower dopant concentration than the buried layer;

a first silicon controlled rectifier device formed in the second active region, the first silicon controlled rectifier device comprising a first well region of the first conductivity type formed in the first semiconductor layer, a first doped region of the first conductivity type formed in the first well region, the buried layer, a second well region of the first conductivity type formed in the first semiconductor layer and spaced apart from the first well region, and a second doped region of the second conductivity type formed in the second well region; and

a second silicon controlled rectifier device comprising the second well region, a third doped region of the first conductivity type formed in the second well region, the buried layer, the first well region, and a fourth doped region of the second conductivity type formed in the first well region, wherein the first and second silicon controlled rectifier devices are coupled to the internal circuitry and form an ESD structure for protecting the internal circuitry against positive and negative ESD stresses.

2. (previously presented): The high frequency integrated circuit structure of claim 1 wherein the body of semiconductor material comprises:

a semiconductor wafer having the first conductivity type; and

a second semiconductor layer formed over the semiconductor wafer, wherein the second semiconductor layer comprises the first conductivity type, and wherein the second semiconductor layer has a lower dopant concentration than the semiconductor wafer, and wherein the buried layer is formed adjacent the second semiconductor layer.

3. (original): The high frequency integrated circuit device of claim 2 further comprising:

a first ohmic contact coupling the first and fourth doped regions; and

a second ohmic contact coupling the second and third doped regions.

4. (previously presented): The high frequency integrated circuit device of claim 2 further comprising a deep contact trench extending from a surface of the first semiconductor layer into the semiconductor wafer.

5. (previously presented): The high frequency integrated circuit device of claim 1 further comprising a field dielectric region formed on a surface of the first semiconductor layer between the first and second wells.

6. (currently amended): The high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a dopant concentration of approximately 1.0×10^{13} atoms/cm^3.

7. (previously presented): the high frequency integrated circuit structure of claim 2, wherein the second semiconductor layer has a thickness from about 1.5 microns to about 3.0 microns.

8. (previously presented): The high frequency integrated circuit structure of claim 1 further comprising a deep isolation trench formed in the body of semiconductor material for isolating the ESD structure from the internal circuitry, wherein the deep isolation trench includes a dielectric layer.

9. (currently amended): A symmetrical SCR device comprising:

a semiconductor substrate of a first conductivity type;

a first semiconductor layer of the first conductivity type formed over the semiconductor substrate, wherein the first semiconductor layer has a lower dopant concentration than the semiconductor substrate;

a second semiconductor layer of a second conductivity type formed adjacent the first semiconductor layer;

a third semiconductor layer of the second conductivity type formed adjacent the second semiconductor layer, wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

first and second wells comprising the ~~second~~ <u>first</u> conductivity type formed in the third semiconductor layer, wherein the first and second wells are spaced apart<u>, and wherein the first and second wells contact the second semiconductor layer</u>;

first and second doped regions formed in the first well, wherein the first doped region comprises the first conductivity type and the second doped region comprises the second conductivity type, and wherein the first and second doped regions are electrically coupled; and

third and fourth doped regions formed in the second well, wherein the third doped region comprises the first conductivity type and the fourth doped region comprises the second conductivity type, and wherein the third and fourth doped regions are electrically coupled.

Claim 10 (cancelled).

11. (currently amended): The SCR device of claim 9 wherein the first semiconductor layer has a dopant concentration of about $1.0x10^{13}$ atoms/cm^3, and a thickness of about 1.5 to about 3.0 microns.

12. (previously presented): The SCR device of claim 9 further comprising a deep isolation trench extending from a surface of the third semiconductor layer into the semiconductor substrate.

13. (previously presented): The SCR device of claim 9 further comprising a deep contact trench extending from a surface of the third semiconductor layer into the semiconductor substrate.

14. (previously presented): The SCR device of claim 9 further comprising an isolation region formed on a surface of the third semiconductor layer between the first and second wells.

15. (previously presented): The SCR device of claim 9 wherein the first conductivity type comprises p-type, and wherein the second conductivity type comprises n-type.

16. (withdrawn): A method for forming a high frequency SCR device including the steps of:

providing a semiconductor substrate including a first semiconductor layer of a first conductivity type, a second semiconductor layer of a second conductivity type over the first semiconductor layer, and a third semiconductor layer over the second semiconductor layer, wherein the third semiconductor layer comprises the second conductivity type, and wherein the third semiconductor layer has a lower dopant concentration than the second semiconductor layer;

forming first and second wells in the third semiconductor layer, wherein the first and second wells comprise the first conductivity type, and wherein the first and second wells are spaced apart;

forming first and second doped regions in the first well, wherein the first doped region comprises the first conductivity type, and the second doped region comprises the second conductivity type; and

forming third and fourth doped regions in the second well, wherein the third doped region comprises the first conductivity type, and wherein the fourth doped region comprises the second conductivity type.

17. (withdrawn): The method of claim 16 wherein the step of providing the semiconductor substrate includes providing a semiconductor substrate having a fourth semiconductor layer formed between the first semiconductor layer and the second semiconductor layer, wherein the fourth semiconductor layer comprises the first conductivity type, and wherein the fourth semiconductor layer has a lower dopant concentration than the first semiconductor layer.

18. (withdrawn): The method of claim 16 further comprising the steps of:

forming an isolation region on a surface of the third semiconductor region between the first and second wells;

forming a first ohmic contact coupling the first and second doped regions; and

forming a second ohmic contact coupling the third and fourth doped regions.

19. (withdrawn): The method of claim 16 further comprising the step of forming a deep isolation trench that surrounds the high frequency SCR device, and that extends from a surface of the third semiconductor layer into the first semiconductor layer.

20. (withdrawn): The method of claim 16 further comprising the step of forming a deep contact trench extending from a surface of the third semiconductor layer into the first semiconductor layer.